# NAGA NANDA SAI PALANKI

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## PROFESSIONAL SUMMARY

Hardware Validation Engineer with 3+ years of hands-on experience in post-silicon bring-up, peripheral/protocol validation, and system-level hardware qualification across PCIe Gen4, I2C, SPI, and UART/USART interfaces. Skilled in Python- and Bash-based test automation on Linux, lab instrumentation (oscilloscopes, logic/protocol analyzers, thermal chambers), and PVT (power/voltage/temperature) qualification testing across EVT/DVT/PVT stages. Experienced in root-cause analysis of hardware-firmware interaction failures and cross-functional collaboration with firmware, design, and platform teams.

## TECHNICAL SKILLS

**Protocols/Interfaces:** PCIe Gen4 (LTSSM, link training, ASPM power states), NVMe (storage device qualification), I2C, SPI, UART/USART, GPIO

**Validation & Test:** Board bring-up, power sequencing, clock/PLL validation, functional & regression testing, fault/error injection, PVT (power/voltage/temperature) margin testing, EVT/DVT/PVT qualification stages, server platform hardware qualification

**Lab Equipment:** Oscilloscopes, logic analyzers, protocol analyzers, DMMs, thermal chambers, power supplies, ST-Link/SWD & JTAG debuggers

**Programming/Automation:** Python (test automation, instrument control, log parsing), Bash/Shell scripting, Embedded C, Linux CLI

**Other:** Root-cause analysis, defect tracking (JIRA), register-level datasheet compliance verification

## PROFESSIONAL EXPERIENCE

**Hardware Validation Engineer** | *Microchip Technology, Austin, TX* **Jul 2025 – Present**

- Performed post-silicon board bring-up on evaluation platforms, including power sequencing, clock validation, and debug connectivity checks.
- Validated PCIe Gen4 link behavior including link training, LTSSM state transitions, and power-management (ASPM) states across multiple endpoint device types including storage controllers and connectivity chips.
- Executed functional and regression testing on I2C, SPI, UART, and GPIO interfaces, including fault and error-injection scenarios.
- Used oscilloscopes, logic analyzers, protocol analyzers, and DMMs to investigate and debug interface and signal-level failures.
- Developed Python and Bash scripts on Linux to automate test execution, control lab instruments via VISA, collect diagnostics, and compare actual vs. expected results across silicon revisions.
- Reproduced and root-caused test failures, capturing waveforms and register-state data in collaboration with firmware and design teams to drive hardware bug resolution.
- Supported EVT/DVT/PVT qualification testing using thermal chambers and voltage margin tools, validating hardware stability across full temperature and voltage operating ranges for production sign-off.

**Hardware Validation Engineer** | *STMicroelectronics, Bangalore, India* **Aug 2021 – Jun 2023**

- Validated I2C, SPI, and UART/USART peripheral interfaces across multiple operating modes and configurations.
- Tested UART in polling, interrupt, and DMA transfer modes across varying baud rates, verifying framing, parity, and overrun error recovery.
- Supported board bring-up including power rail checks, oscillator/PLL behavior, clock distribution, and SWD/JTAG debug connectivity.
- Captured and analyzed I2C, SPI, and UART waveforms, comparing register states to isolate firmware, configuration, board, or silicon-level issues.
- Developed Python, Bash, and Embedded C scripts on Linux to automate repetitive validation and regression testing, and analyzed failure logs for recurring defect patterns across successive silicon tape-outs.

## EDUCATION

**M.S. in Computer Science** — University of North Texas **Aug 2023 – May 2025**

**B.Tech in Electronics and Communication Engineering** — LBRCE, India **Jun 2017 – May 2021**